REMARKS

In light of the following remarks, reconsideration of the present application is respectfully requested. Claims 1-26 are pending in this application. Claims 1, 10, 17 and 22 are independent claims. No new matter has been added.

Applicant wishes to thank the Examiner for his time during the telephonic interview of December 22, 2008. During the interview, Applicant and the Examiner discussed the merits of claim 1 relative to a second cache memory for providing at least one second instruction to the DSP core when the running flag signal is disabled. In more detail, Applicant primarily set forth arguments commensurate with those shown below. At the conclusion of the interview, the Examiner agreed that upon initial review, the references do not disclose, "a second cache memory for providing at least one second instruction to the DSP core when the running flag signal is disabled," as recited in original claim 1. The Examiner suggested that Applicant file a response in accordance with the arguments set forth during the interview.

Allowable Subject Matter

As indicated by the Examiner, claims 5-9, 12-16, 20-21 and 24 define allowable subject matter. However, as all claims are believed to be allowable, these claims have merely been maintained in their current form.

Rejections Under 35 U.S.C. § 103

1. Claims 1-4, 17-19, 22, 23 and 26 stand rejected under 35 U.S.C. §103(a) as being obvious over Morikawa et al. (US 2001/0032297), hereinafter "Morikawa," in

view of Arimilli et al. (US 2002/0087815), hereinafter "Arimilli." Applicant respectfully traverses this rejection for the reasons detailed below.[1]

Claim 1 requires, inter alia, "a second cache memory for providing at least one second instruction to the DSP core when the running flag signal is disabled." At least this feature is not disclosed or suggested by Morikawa, Arimilli or a combination of the two (assuming *arguendo* that they can be combined, which Applicant does not admit).

Morikawa discloses a cache memory apparatus including a processor 1, a lower-level memory 9 and a cache apparatus 5 having a naked cache 6 and a cache-miss cache memory 7, as shown in FIG. 2 of Morikawa. FIG. 2 is reproduced below.

FIG. 2

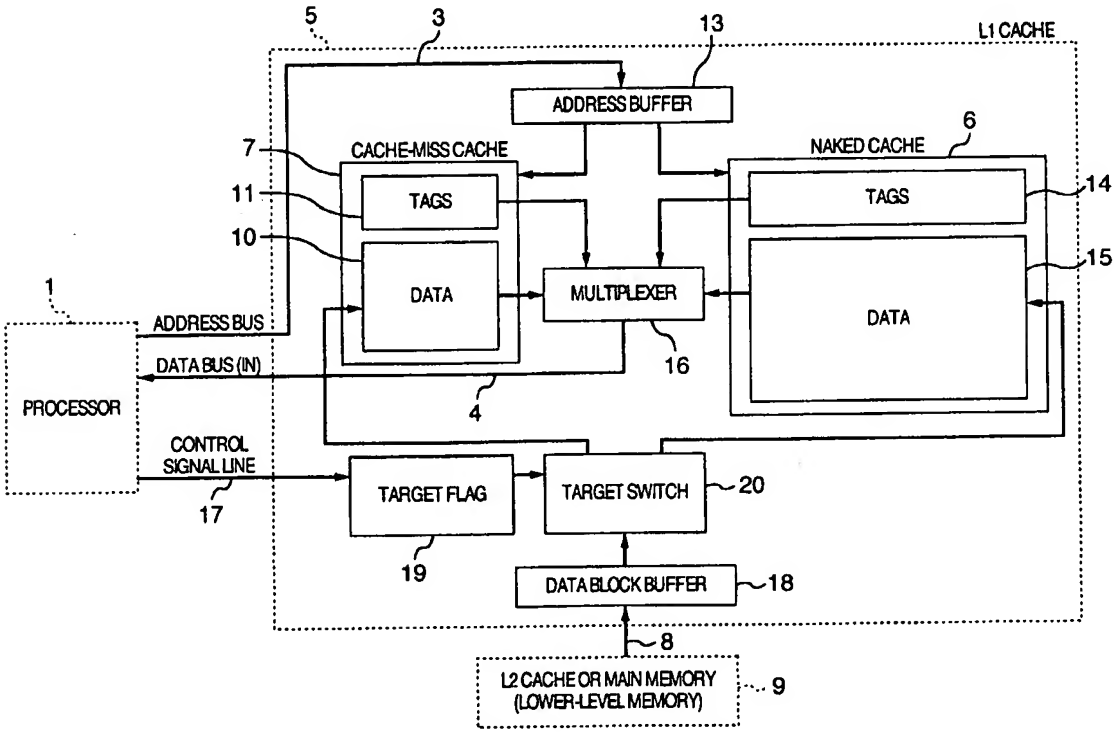

FIG. 2 of Morikawa.

[1] To be thorough, further expedite prosecution, and for the sake of clarity, Applicants provide discussions throughout this Request for Reconsideration of each of the references separately. However, Applicants are not attacking these references individually, but arguing that the references, even taken in combination, fail to render the claimed invention obvious because all features are not found in the prior art.

A target flag 19 holds storage destination cache information. During a prefetch instruction that produces a cache-miss, processor 1 sets target flag 19 to "0" via a control signal line 17 and orders the data to be stored in naked cache memory 6. If it is not a prefetch instruction and there has been a cache-miss in both naked cache memory 6 and cache-miss cache memory 7, processor 1 sets target flag 19 to "1" via control signal line 17 and orders the data to be stored in cache-miss cache memory 7.

The Examiner relies on the cache-miss memory 7 of Morikawa to teach the "second cache memory," of claim 1. Moreover, the Examiner asserts that the setting of target flag 19 to "1" of Morikawa et al. corresponds to the "disabling the running flag signal," of claim 1. However, when the target flag 19 is set to "1," the cache-miss cache memory 7 receives an instruction from processor 1. Accordingly, cache-miss cache memory 7 is not a second cache memory that provides "at least one second instruction to the DSP core when the running flag is disabled," as required by claim 1. By contrast, cache-miss memory 7 of Morikawa receives an instruction from processor 1.

Applicant respectfully submits that even assuming for the sake of argument that Morikawa and Arimilli can be properly combined (which Applicant does not admit), Arimilli fails to disclose the deficiencies of Morikawa discussed above and, therefore, claim 1 is not rendered obvious by a combination of Morikawa and Arimilli. Claims 2-4, which are dependent upon claim 1, are patentable for at least the reasons set forth above regarding claim 1.

Claim 17 requires, inter alia, "a third cache memory which provides a third instruction to the DSP core in response to the first miss signal, when the running flag signal is disabled." Applicant submits that at least this feature is not disclosed by

Morikawa, Arimilli or a combination of the two (assuming they can be properly combined, which Applicant does not admit).

Claim 22 requires, inter alia, "providing a third instruction from a third cache memory to the DSP core in response to the program address based on ... a disabling of the running flag signal by the second cache memory." Applicant submits that at least this feature is not disclosed by Morikawa, Arimilli or a combination of the two (assuming they can be properly combined, which Applicant does not admit).

Moreover, claims 17 and 22 are separate independent claims from claim 1, wherein each independent claim contains its own individual limitations. Each independent claim should be interpreted solely based upon limitations set forth therein. However, claims 17 and 22 are patentable for at least reasons somewhat similar to those set forth above regarding claim 1. Claims 18, 19, 23 and 26, which are dependent on claims 17 or 22, are patentable for at least the reasons set forth above.

For at least the foregoing reasons, Applicant respectfully requests that the rejections of these claims be withdrawn.

2. Claims 10, 11, 13 and 25 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Morikawa in view of Arimilli and Chiu et al. (US 6,505,253), hereinafter "Chiu." Applicant respectfully traverses this rejection for the reasons detailed below.

Claim 10 requires, inter alia, "disabling the running flag signal and ceasing said second providing step when the given number of instructions reaches a threshold value."

As described above, Morikawa in view of Arimilli does not disclose or suggest the "second cache memory for providing at least one second instruction to the DSP core when the running flag signal is disabled," of claim 1. Therefore, Applicant submits that Morikawa and Arimilli, either alone or in combination (assuming they can be properly combined, which Applicant does not admit), do not disclose or suggest the "disabling the running flag signal and ceasing said second providing step when the given number of instructions reaches a threshold value," of claim 10.

Moreover, Applicant respectfully submits that even assuming for the sake of argument that Morikawa, Arimilli and Chiu can be properly combined (which Applicant does not admit), Chiu fails to disclose the deficiencies of Morikawa and Arimilli discussed above and, therefore, claim 10 is not rendered obvious by a combination of Morikawa, Arimilli and Chiu. Claims 11, 13 and 25, which are dependent on claim 10, are patentable for at least the reasons set forth above.

Therefore, Applicant respectfully requests that the Examiner withdraw this rejection.

CONCLUSION

In view of the above remarks and amendments, Applicant respectfully submits that each of the rejections has been addressed and overcome, placing the present application in condition for allowance. A notice to that effect is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to contact the undersigned.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact John A. Castellano at the telephone number of the undersigned below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By _____

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